## REMARKS

By this Amendment, claims 1 and 7 are amended to broaden and clarify the allowable recited subject matter, claims 5 and 6 are cancelled without prejudice or disclaimer and the specification is amended merely to correct the phrase "blank deposition" to "blanket deposition" throughout the specification. Claims 1-4 and 7-8 are pending.

The Office Action rejected claims 1-2 and 5-8 under 35 U.S.C. 102 as being anticipated by Adamic (U.S. 6,124,179) and rejected claims 1, 3 and 4 under 35 U.S.C. 102 as being anticipated by Boggs et al. (U.S. 6,444,487; hereafter "Boggs"). Applicant traverses the rejections because the cited prior art references, analyzed individually or in combination, fail to disclose, teach or suggest all the features recited in the rejected claims. For example, the cited prior art fails to disclose, teach or suggest, the method of **forming a lateral power semiconductor device** having an active region that includes a drift region, the method comprising forming, in a layer provided on a semiconductor substrate, a power semiconductor device having an active region that includes a drift region; removing at least a portion of the semiconductor substrate below at least a portion of the drift region **such that said at least a portion of the drift region is provided in a membrane defined by that portion of the layer below which the semiconductor substrate has been removed; and providing electrical contacts on only one surface of the power semiconductor device**," as recited in independent claim 1 and its dependent claims.

Ademic merely teaches vertical devices, in which there are electrical contacts at opposite surfaces (by convention called the top and bottom surfaces, or frontside and backside surfaces). Such devices are fundamentally different then lateral devices, wherein there are electrical contacts on only one surface (by convention called the top or frontside surface). Thus, for example, Ademic teaches on the subject of vertical devices at column 1, lines 30 to 44, column 3, lines 19 to 21; and the entirety of the specific description from column 4, line 7 onwards. More specifically, column 9, lines 28 to 62, contains a description of the formation of the top or frontside electrical contacts. Likewise, the formation of the bottom or backside electrical contacts is described at column 13, line 66 to column 14, line 23 and column 14, lines 64 to 66. Thus, the description and correspondingly the drawings of Ademic are almost exclusively in relation to vertical devices.

Moreover, the disclosure of Ademic focuses on improving the operation of vertical devices. As is clearly explained at for example column 1, lines 31 to 33 of Ademic, performance of vertical transistors is improved by reducing the collector or drain leadout

resistance. The object of the invention of Ademic is to reduce this leadout resistance. As mentioned at column 2, lines 54 to 60 and column 3, lines 12 to 16, this is done by incorporating a conductive layer in close proximity to an active collector or drain region. To achieve this, it is explained at column 12, lines 1 to 8 that the silicon wafer 201 in Figure 2C under the semiconductor devices is removed. Column 13, lines 66 onwards describes that a conductive layer 256 is deposited on the exposed portions of the backside surface. The bottom or backside electrical connections are then made. Thus, the whole purpose of Ademic is to reduce the leadout resistance at the bottom or backside connections of a vertical device, and this is achieved by removing substrate from the bottom surface and introducing an electrically conductive layer to which the bottom electrical contacts of the vertical device are made.

However, there is no motivation in Ademic to remove the substrate below at least a portion of the drift region of a lateral device. The purpose of removing the substrate under the drift region in the vertical devices of Ademic was to allow a better electrical contact at the bottom or backside surface of the device, which is only relevant for vertical devices. Given that there would be no such advantage for lateral devices, in which all electrical contacts are at the top or frontside surface and in which there are no electrical contacts to the bottom or backside surface, one of ordinary skill in the art would not have been motivated by Ademic to remove the substrate in a lateral device.

Thus, one of ordinary skill in the art would have been motivated by Ademic to remove the substrate below at least a portion of the drift region of a lateral device because Ademic provides no teaching or suggestion regarding such removal in lateral devices. Therefore, one of ordinary skill in the art would not have understood that any advantage would be provided by such a removal because Ademic fails to disclose, teach or suggest it in lateral devices.

Accordingly, Ademic fails to disclose, teach or suggest the claimed method of forming a lateral power semiconductor device, including removing at least a portion of the semiconductor substrate below at least a portion of the drift region such that said at least a portion of the drift region is provided in a membrane defined by that portion of the layer below which the semiconductor substrate has been removed; and providing electrical contacts on only one surface of the power semiconductor device, as recited in independent claim 1 and its dependent claims.

Boggs fails to remedy this deficiency of Ademic because Boggs merely discloses a semiconductor strain sensor in which the substrate of the device is thinned to make the device flexible, which is relevant given that it is used as a strain sensor. However, power devices are not used as strain sensors. Therefore Boggs offers no motivation to remove the substrate in a power device. Thus, Boggs fails to disclose a power semiconductor device. Because the devices of Boggs are not power semiconductor devices, they do not have a drift region. Accordingly, Boggs also fails to disclose teach or suggest removing a substrate under a lateral device to provide enhanced breakdown ability due to a more favorable electric field and potential distribution within the drift region of the lateral power device.

Accordingly, the combined teachings of Ademic and Boggs fail to disclose, teach or suggest the claimed method of forming a lateral power semiconductor device, including removing at least a portion of the semiconductor substrate below at least a portion of the drift region such that said at least a portion of the drift region is provided in a membrane defined by that portion of the layer below which the semiconductor substrate has been removed; and providing electrical contacts on only one surface of the power semiconductor device, as recited in independent claim 1 and its dependent claims.

All objections have been addressed. If anything further is necessary to place the application in condition for allowance, Applicant requests that the Examiner contact Applicant's undersigned representative at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
PILLSBURY WINTHROP LLP

CHRISTINE H. MCCARTHY
Reg. No. 41844
Tel. No. 703. 905.2143
Fax No. 703 905.2500

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P.O. Box 10500
McLean, VA 22102
(703) 905-2000